**Industrial Monitoring System Test Plan**

**Fiber Optic System**

* Test with a signal generator input, starting at a low data rate, and increasing until signal is no longer clear on the other end (also using varying duty cycles to simulate varying input)

**Manchester Encode/Decode**

* Test using a signal generator, checking and comparing input vs. output using scope (vary the duty cycle to check and confirm output still consistend)
* Add in fiber optic system in between encoder/decoder and confirm that the data stream is still visibly decoded on the other end

**Time Division Multiplexed Frames**

* Test sending directly from one Altera board to the other using an external clock
  + Test with various frame inputs and confirm they are still being received
  + Test injecting errors into the frame and confirming they are being recorded as errors on the receiving end
* Test transmitting frames through Manchester Encode/Decode and Fiber systems
  + Run using clocking from Manchester chips

**Sensor testing**

* Test ADC output using LED’s, with varying conversion rates
* Test receiving the ADC input in parallel onto the Altera board and confirm no errors
* Transmit TDM frames filled with correct sensor data over the whole network

**TDM Frame Reception**

A frame will not be received unless it starts with the 9 bit high sync sequence, so any incorrect frames

with an error in the sync sequence will not be received. After the sync sequence has been received, 27

more bits will be received (3 Bytes each followed by an injected low bit to ensure the sync sequence

isn’t found). After the 27 bytes have been received, the final byte (checksum) is compared to the XOR of

the first two bytes to verify that the frame is valid. If errors are detected, the frame is discarded and the

error is recorded. Otherwise, the Altera board will display the output on both the 7 segment displays

and the monitor. To test and verify reception of correct frames and ensure detection of errors, we will

implement a switch on the transmit board to inject errors into a frame, and then we will slow the data

rate to be able to send a series of correct, incorrect, or intermixed correct and incorrect frames.

**TDM State Diagram**